IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.(Currently Amended) An active matrix device comprising an array of display pixels, each pixel comprising:

a current driven light emitting display element ~~(2)~~;

an amorphous silicon drive transistor ~~(T_D)~~ for driving a current through the display element;

first and second capacitors ~~(C_1, C_2)~~ connected in series between ~~the~~ gate and source or drain of the drive transistor, a data input to the pixel being provided to ~~the~~ a junction between the first and second capacitors ~~(C_1, C_2)~~ thereby to charge the second capacitor ~~(C_2)~~ to a voltage derived from ~~the~~ a pixel data voltage associated with the data input, and a voltage derived from ~~the~~ a drive transistor threshold voltage being stored on the first capacitor ~~(C_1)~~; and

a further transistor connected across terminals of the second capacitor.

2.(Currently Amended) ~~A~~ The device as claimed in claim 1, wherein each pixel further comprises an input first transistor ~~(A_1)~~ connected between an input data line ~~(32)~~ and the junction between the first and second capacitors ~~(C_1, C_2)~~.

3.(Currently Amended) ~~A~~ The device as claimed in claim 1, wherein the drain of the drive transistor ~~(T_D)~~ is connected to a power supply line ~~(26)~~.

4.(Currently Amended) ~~A~~ The device as claimed in claim 1, wherein each pixel further comprises a second transistor ~~(A_2)~~ connected between the gate and drain of the drive ~~transistor~~ transistor.

5.(Currently Amended) ~~A~~ The device as claimed in claim 4, wherein the second transistor ~~(A_2)~~ is controlled by a first gate control line which is shared between a row of pixels.

6.(Currently Amended) ~~A~~ The device as claimed in claim 1, wherein the first and second capacitors ~~(C_1, C_2)~~ are connected in series between the gate and source of the drive transistor ~~(T_D)~~.

Claim 7 (Canceled)

8.(Currently Amended) ~~A~~ The device as claimed in ~~claim 7~~ claim 1, wherein the ~~third~~ further transistor is controlled by a ~~third~~ further gate control line which is shared between a row of pixels.

9.(Currently Amended) ~~A~~ The device as claimed in ~~claim 8~~ claim 5, wherein the further transistor is controlled by a further gate control line, and the ~~second~~ first and ~~third~~ further gate control lines comprise a single shared control line.

10.(Currently Amended) ~~A~~ The device as claimed in claim 1, wherein the first and second capacitors ~~(C_1, C_2)~~ are connected in series between the gate and drain of the drive transistor ~~(T_D)~~.

11. (Currently Amended) ~~A device as claimed in claim 10, wherein each pixel further comprises a third~~ An active matrix device comprising an array of display pixels, each pixel comprising:

a current driven light emitting display element;

an amorphous silicon drive transistor for driving a current through the display element;

first and second capacitors connected in series between gate and source or drain of the drive transistor, a data input to the pixel being provided to a junction between the first and second capacitors thereby to charge the second capacitor to a voltage derived from a pixel data voltage associated with the data input, and a voltage derived from a drive transistor threshold voltage being stored on the first capacitor; and

a further transistor ~~(A_3)~~ connected between the ~~input~~ gate and the source of the drive transistor ~~(T_D)~~.

12. (Currently Amended) ~~A~~ The device as claimed in claim 11, wherein the ~~third~~ further transistor ~~(A_3)~~ is controlled by a ~~third~~

further gate control line which is shared between a row of pixels.

Claim 13 (Canceled)

14. (Currently Amended) ~~A~~ The device as claimed in claim 1, wherein each pixel further comprises a ~~fourth~~ switching transistor ~~(A_4)~~ connected between the drive transistor source and a ground potential line.

15. (Currently Amended) ~~A~~ The device as claimed in claim 14, wherein the ~~fourth~~ transistor ~~(A_4)~~ is controlled by a ~~fourth~~ switching gate control line which is shared between a row of pixels.

16. (Currently Amended) ~~A~~ The device as claimed in claim 15, wherein the ground potential line is shared between a row of pixels and comprises the ~~fourth~~ switching gate control line for the ~~fourth~~ switching transistors of an adjacent row of pixels.

17. (Currently Amended) ~~A~~ device as claimed in claim 1,

wherein ~~the~~ a capacitor arrangement ~~(C_1, C_2)~~ including the first and second capacitors is connected between the gate and source of the drive transistor ~~(T_D)~~, and the source of the drive transistor is connected to a ground line.

18. (Currently Amended) ~~A~~ The device as claimed in claim 17, wherein the drain of the drive transistor ~~(T_D)~~ is connected to one terminal of the display element ~~(2)~~, the other terminal of the display element being connected to a power supply line.

19. (Currently Amended) ~~A device as claimed in claim 17, wherein each pixel further comprises~~ An active matrix device comprising an array of display pixels, each pixel comprising:

a current driven light emitting display element;

an amorphous silicon drive transistor for driving a current through the display element;

first and second capacitors connected in series between gate and source or drain of the drive transistor, wherein the source of the drive transistor is connected to a ground line, a data input to the pixel being provided to a junction between the first and second

capacitors thereby to charge the second capacitor to a voltage derived from a pixel data voltage associated with the data input, and a voltage derived from a drive transistor threshold voltage being stored on the first capacitor; and

a ~~second~~ shorting transistor ~~(A_2)~~ connected across ~~the~~ terminals of the second capacitor ~~(C_2)~~.

20. (Currently Amended) ~~A~~ The device as claimed in claim 17, wherein each pixel further comprises a ~~third~~ further transistor ~~(A_3)~~ connected between the gate and drain of the drive transistor.

21. (Currently Amended) ~~A~~ The device as claimed in claim 20, wherein the ~~third~~ further transistor ~~(A_3)~~ is controlled by a gate control line which is shared between a row of pixels.

22. (Currently Amended) ~~A device as claimed in claim 17, wherein each pixel further comprises a fourth~~ An active matrix device comprising an array of display pixels, each pixel comprising:

a current driven light emitting display element;

an amorphous silicon drive transistor for driving a current through the display element;

first and second capacitors connected in series between gate and source or drain of the drive transistor, a data input to the pixel being provided to a junction between the first and second capacitors thereby to charge the second capacitor to a voltage derived from a pixel data voltage associated with the data input, and a voltage derived from a drive transistor threshold voltage being stored on the first capacitor; and

a charging transistor ~~(A_4)~~ connected between a power supply line ~~(50)~~ and the drain of the drive transistor.

23. (Currently Amended) ~~A~~ The device as claimed in claim 1, wherein each pixel further comprises a second drive transistor ~~(T_2)~~.

24. (Currently Amended) ~~A~~ The device as claimed in claim 23, wherein the second drive transistor is provided between a power supply line ~~(26)~~ and the first drive transistor ~~(T_D)~~.

25. (Currently Amended) ~~A~~ The device as claimed in claim 24, wherein the gate and drain of the second drive transistor are connected together.

26. (Currently Amended) ~~A~~ The device as claimed in claim 23, wherein the second drive transistor is provided between the first drive transistor ~~(T_D)~~ and the display element ~~(2)~~.

27. (Currently Amended) ~~A~~ The device as claimed in claim 26, wherein ~~a~~ another transistor ~~(A_5)~~ is connected between the gate and drain of the second drive transistor ~~(T_S)~~.

28. (Currently Amended) ~~A~~ The device as claimed in claim 26, wherein each pixel further comprises ~~a fourth~~ another transistor ~~(A_4)~~ connected between the gate of the second drive transistor ~~(T_S)~~ and a ground potential line.

29. (Currently Amended) ~~A~~ The device as claimed in claim 1, wherein the drive transistor ~~(T_D)~~ comprises an n-type transistor.

30. (Currently Amended) ~~A~~ The device as claimed in claim 1, wherein the display element comprises an electroluminescent ~~(EL)~~ display element.

31. (Currently Amended) ~~A~~ The device as claimed in claim 30, wherein the electroluminescent ~~(EL)~~ display element comprises an electrophosphorescent organic electroluminescent display element.

32. (Currently Amended) A method of driving an active matrix display device comprising an array of current driven light emitting display pixels, each pixel comprising an display element ~~(2)~~ and an amorphous silicon drive transistor ~~(T_D)~~ for driving a current through the display element, the method comprising, for each pixel:

driving a current through the drive transistor ~~(T_D)~~ to ground, and charging a first capacitor ~~(C_1)~~ to the resulting gate-source voltage;

discharging the first capacitor ~~(C_1)~~ until the drive transistor turns off, the first capacitor thereby storing a threshold voltage;

charging a second capacitor ~~(C_2)~~, in series with the first

capacitor between the gate and source or drain of the drive transistor, to a data input voltage; and

using the drive transistor ~~(T_D)~~ to drive a current through the display element using a gate voltage that is derived from the voltages across the first and second capacitors ~~(C_1, C_2)~~.

33. (Currently Amended) ~~A~~ The method as claimed in claim 32, wherein the step of charging a second capacitor is carried out by switching on an address transistor ~~(A1)~~ connected between a data line and an input to the pixel.

34. (Currently Amended) ~~A~~ The method as claimed in claim 33, wherein the address transistor for each pixel in a row is switched on simultaneously by a common row address control line.

35. (Currently Amended) ~~A~~ The method as claimed in claim 34, wherein the address transistors for one row of pixels are turned on substantially immediately after the address transistors for an adjacent row are turned off.

36. (Currently Amended) ~~A~~ The method as claimed in claim 32, wherein the first capacitor ~~(C_1)~~ of each pixel is charged to store a respective threshold voltage of the pixel drive transistor at an initial threshold measurement period of a display frame period, a pixel driving period of the frame period following the threshold measurement period.